METHOD FOR FORMING A SELF-ALIGNED CONTACT HOLE IN A SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a method for forming a self-aligned contact hole. More particularly, the present invention relates to a method for forming contact holes between closely disposed conductive structures on a substrate using a self-aligning process.

2. Description of the Related Art

[0002] As semiconductor devices become more highly integrated and are required to have higher response speeds, patterns formed on a substrate must become increasingly minute. More particularly, a width of a pattern and a space between adjacent patterns are being greatly reduced. Specifically, since a contact should be formed to connect isolated devices on a semiconductor substrate to a highly conductive film, while an aligning margin and an isolation margin are maintained, the contact occupies a significant area on the semiconductor substrate. Accordingly, dimensions of the contact greatly affect the overall size of a memory device in which identical cells are repeatedly formed, such as a dynamic random access

memory (DRAM), a static random access memory (SRAM) or a non-volatile memory (NVM).

[0003] Recently, a contact having a minute size has not been able to be exactly formed using conventional semiconductor manufacturing methods even though the semiconductor technology has been rapidly developed to form a line width of below approximately 0.25 μm. In addition, heights of conductive film patterns have increased in order to reduce resistances of the conductive film patterns as widths of the conductive film patterns have decreased. As a result, formation of a contact between the conductive film patterns becomes increasingly difficult. Hence, in a case that a design rule does not have a sufficient margin and patterns having identical shapes are repeatedly formed, such as in a memory device, a method for forming a contact hole using a self-aligning process has been developed to reduce the overall area of the device.

[0004] FIGS. 1A to 1E illustrate cross-sectional views of stages in a conventional method for forming a self-aligned contact hole.

[0005] Referring to FIG. 1A, after a conductive film is formed on a substrate 10, a nitride film is formed on the conductive film. Then, portions of the

nitride film and the conductive film are etched to expose the substrate 10 so that conductive structures 15 including conductive film patterns 12 and nitride film patterns 14 are formed on the substrate 10.

[0006] Referring to FIG. 1B, a nitride film is uniformly formed on the conductive structures 15 and on the substrate 10. The nitride film is then anisotropically etched so that the nitride film remains at sidewall portions of the conductive structures 15, thereby forming nitride spacers 16. Here, upper portions of the nitride film patterns 14 on the conductive film patterns 12 are partially etched while the nitride film on the substrate 10 is completely removed. Thus, the upper portions of the nitride film patterns 14a have rounded shapes.

[0007] Referring to FIG. 1C, an insulation film 18 including silicon oxide is formed to fill a space between the conductive structures 15 including the nitride spacers 16.

[0008] Referring to FIG. 1D, using an anisotropic etching process having an etching selectivity between silicon oxide and silicon nitride, a predetermined portion of the insulation film 18 is etched to form a preliminary contact hole exposing a portion of the substrate 10 between the conductive structures 15

including the nitride spacers 16a. When the insulation film 18 is etched to expose the portion of the substrate 10 between the conductive structures 15 having the nitride spacers 16, an upper portion of the nitride spacers 16a is etched in accordance with a ratio corresponding to the etching selectivity.

[0009] Referring to FIG. 1E, the substrate 10 and the resultant structures formed thereon are rinsed with a rinsing chemical to remove polymers generated during the etching so that self-aligned contact holes 20 are formed. When the substrate 10 is rinsed, an exposed portion of the etched insulation film 18a is partially etched.

[0010] As the patterns become much smaller to meet demand of high integration of semiconductor devices, several disadvantages of this conventional method for forming the self-aligned contact hole become apparent.

[0011] First, a thickness of the nitride spacer 16 should be reduced so that a space between the conductive structures 15 may be significantly decreased. When the nitride spacer 16 has a relatively large thickness, the space between the conductive structures 15 becomes so narrow that the insulation film 18 may not be able to completely fill in the space. In addition, a

parasitic capacitance may be increased due to the nitride spacer 16. Alternately, when the thickness of the nitride spacer 16 decreases, the conductive film pattern 12 covered by the nitride spacer 16 may be easily exposed because the nitride spacer 16 may be consumed during formation of the self-aligned contact hole 20. As a result, a bridge failure frequently occurs between the conductive film pattern 12 and conductive materials filling the self-aligned contact hole 20.

[0012] Second, upper side, or "shoulder," portions of the nitride spacers 16a become increasingly rounded as widths of the conductive structures 15 decrease. When the shoulder portions of the nitride spacers 16a have more rounded shapes, predetermined portions of the nitride spacers 16 and the nitride film patterns 14a are rapidly etched during the formation of the self-aligned contact hole 20, so the conductive film patterns 12 covered by the nitride spacers 16 may be exposed.

[0013] Third, a depth of the contact hole 20 necessarily increases as the heights of the conductive structures 15 increase. Thus, a process failure such as a non-opening of a contact may increase.

[0014] Fourth, a remaining portion of the etched insulation film 18a on the nitride spacer 16 significantly decreases as the space between adjacent conductive structures 15 decreases. Further, the remaining portion of the etched insulation film 18a may be completely removed during subsequent processes. Hence, a process failure frequently occurs wherein the conductive materials filling the contact holes 20 are connected to each other during the subsequent processes.

SUMMARY OF THE INVENTION

[0015] The present invention has been made in an effort to solve the aforementioned problems and accordingly, it is a feature of an embodiment of the present invention to provide a method of forming a self-aligned contact hole that is able to minimize process failures.

[0016] In order to provide this feature of an embodiment of the present invention, there is provided a method for forming a self-aligned contact hole including (a) forming a plurality of conductive structures on a semiconductor substrate, each conductive structure including a conductive film pattern having an upper and side surfaces and a protection pattern formed on the upper and surfaces of the conductive film pattern; (b) forming a first

insulation film to fill a space between adjacent conductive structures; (c) successively etching upper portions of the first insulation film and the protection patterns until each of the protection patterns has a level upper surface that is exposed; (d) forming a second insulation film on the resultant structure on the semiconductor substrate; and (e) selectively etching portions of the second insulation film and the first insulation film using a photolithography process to form the self-aligned contact hole exposing a portion of the semiconductor substrate between adjacent conductive structures.

[0017] In one embodiment of the present invention, the successive etching results in the first insulation film being etched slower than the protection pattern so that a portion of the first insulation film filled between adjacent conductive structures protrudes from the upper surface of the conductive structures.

[0018] The method of the present invention may further include forming a nitride liner on the plurality of conductive structures and on the semiconductor substrate after forming the plurality of conductive structures.

In addition, the method preferably includes forming a conductive material in the self-aligned contact hole to form a contact.

[0019] According to the present invention, a process failure, such as a non-opening of the contact, may be prevented because protection patterns have level upper surfaces, and the protection patterns have heights lower than conventional protection patterns. In addition, consumption of the protection patterns may be reduced during etching to form a contact hole because an etching selectivity between the protection pattern and the first and second insulation films is enhanced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] The above and other features and advantages of the present invention will become more apparent to those of ordinary skill in the art by describing in detail preferred embodiments thereof with reference to the attached drawings in which:

[0021] FIGS. 1A to 1E illustrate cross-sectional views of stages in a conventional method for forming a self-aligned contact hole of a semiconductor device;

[0022] FIGS. 2A to 2H illustrate cross-sectional views of stages in a method for forming a self-aligned contact hole of a semiconductor device according to a first embodiment of the present invention;

[0023] FIGS. 3A to 3C illustrate cross-sectional view structures depicting an etching selectivity of a structure including silicon oxide and silicon nitride under identical etching conditions; and

[0024] FIGS. 4A to 4E illustrate cross-sectional views of stages in a method for forming a self-aligned contact hole of a semiconductor device according to a second embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0025] Korean Patent Application No. 2002-39138, filed on July 6, 2002, and entitled: "Method for Forming a Self-Aligned Contact Hole in a Semiconductor Device," is incorporated by reference herein in its entirety.

[0026] The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. The invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so

that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. It will also be understood that when a layer is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present. Like numbers refer to like elements throughout.

First Embodiment

[0027] FIGS. 2A to 2H illustrate cross-sectional views of stages in a method for forming a self-aligned contact of a semiconductor device according to a first embodiment of the present invention. In the first embodiment, a self-aligned contact represents a contact formed between gate electrodes in order to make contact with a source region or a drain region.

[0028] Referring to FIG. 2A, a semiconductor substrate 100 is divided into an active region and a field region by forming a field oxide film (not shown) on the substrate 100. The field oxide film may be formed through an isolation process, such as an improved local oxidation of silicon (LOCOS) process or a trench field isolation process.

[0029] Then, a conductive film 102 used for a gate electrode is formed on a gate oxide film (not shown) after the gate oxide film having a thickness of approximately 30 to 100 Å is formed on the semiconductor substrate 100. The conductive film 102 has a polycide structure in which a polysilicon film 102a doped with an impurity having a high concentration is formed on the gate oxide film, and a metal silicide film 102b, preferably a tungsten silicide film, having a thickness of approximately 1,500 Å is formed on the polysilicon film 102a. The polysilicon film 102a having a thickness of approximately 1,000 Å is generally formed using a doping process, such as a diffusion process, an ion implantation process or an in-situ doping process.

[0030] Subsequently, a first silicon nitride film 104 is formed on the conductive film 102 to have a thickness of approximately 1,800 to 2,000 Å. The first silicon nitride film 104 functions as a hard mask when the conductive film 102 is etched in a successive process. In addition, the first silicon nitride film 104 protects the conductive film 102 so that the conductive film 102 is not exposed when successive processes are performed. As an alternative, instead of a first silicon nitride film 104, any film having an

etching selectivity with respect to silicon oxide may be formed on the conductive film 102 under a specific etching process.

[0031] Referring to FIG. 2B, predetermined portions of the first silicon nitride film 104, the conductive film 102 and the gate oxide film are successively etched to form gate structures 106 each including a gate oxide film pattern (not shown), a conductive film pattern 103 and a first silicon nitride film pattern 105. Subsequently, impurities are implanted into the active region of the semiconductor substrate 100 using the gate structures 106 as a mask, thereby forming a source/drain region (not shown) in the active region. Each of the resultant gate structures has a thickness that is greater than approximately 4000 Å.

[0032] Referring to FIG. 2C, a second silicon nitride film (not shown) having a thickness of approximately 1,300 Å is uniformly formed on the gate structures 106 and the semiconductor substrate 100. Subsequently, the second silicon nitride film is anisotropically etched so that the second silicon nitride film remains at a side portion of the gate structures 106. Thus, a nitride spacer 108 is formed at the side portion of the gate structures 106. As the second silicon nitride film formed on a surface of the semiconductor

substrate 100 is completely removed when the second silicon nitride film is anisotropically etched, portions of the second silicon nitride film on the gate structures 106 are also completely removed. In addition, an upper portion of the first silicon nitride film pattern 105a formed on the conductive film pattern 103 is partially etched. Particularly, an upper edge portion of the first silicon nitride film pattern 105a is more etched than an upper central portion of the first silicon nitride film pattern 105a, so an upper surface of the first silicon nitride film pattern 105 has a rounded shape in a sectional view, as shown in FIG. 2C.

[0033] According to the above-described processes, an upper surface and a side surface of the conductive film pattern 103 functioning as the gate electrode are capped with the first silicon nitride film pattern 105a.

[0034] Hereinafter, it will be described that a second silicon nitride pattern 110 includes the nitride spacer 108 and the rounded first silicon nitride film pattern 105a capping the conductive film pattern 103.

[0035] As the integration density of the semiconductor devices greatly increases, the width of the gate electrode becomes significantly smaller. In addition, a space between adjacent gate electrodes is significantly reduced.

In particular, a width of the gate structures 106 is reduced to below approximately 2500 Å, and also a space between adjacent gate structures 106 is decreased to below approximately 1500 Å. In a case that the gate structures 106 have such a small dimension, a boundary portion (that is, the shoulder portion) between an upper surface and a side surface of the second silicon nitride pattern 110 has an increasingly rounded shape. When the shoulder portion of the second silicon nitride pattern 110 has an increasingly rounded shape, the etching selectivity between the silicon nitride film and the silicon oxide film is reduced at the shoulder portion. That is, the conductive film pattern 103 may be exposed because the silicon nitride at the shoulder portion, as well as the silicon oxide, are rapidly etched under an etching condition for selectively etching the silicon oxide.

[0036] Subsequently, a nitride liner 112 having a thickness of approximately 50 to 300 Å is formed on the resultant structure. The nitride liner 112 functions as an etching stop layer during a successive process.

[0037] Referring to FIG. 2D, a first insulation film 114 is formed on the semiconductor substrate 100 to cover the conductive pattern 103 capped with the second silicon nitride pattern 110. As each of the resultant

structures, including the conductive film pattern 103 and the second silicon nitride pattern 110, has a relatively large height of approximately 5,000 Å and an interval between adjacent resultant structures has a relatively small value of below approximately 1,000 Å, it is difficult for the first insulation film 114 to completely fill the space between adjacent resultant structures. Hence, the first insulation film 114 is formed using an oxide having a good reflow-ability, such as boro-phosphor silicate glass (BPSG), undoped silicate glass (USG) or spin-on glass (SOG) in order to fill a gap between adjacent resultant structures.

[0038] Referring to FIG. 2E, upper portions of the first insulation film 114 and the second silicon nitride film pattern 110 are successively etched so that the etched second silicon nitride film pattern 110a has a level upper surface. At that time, the etched first insulation film 114a is higher than the etched second silicon nitride film pattern 110a. That is, portions of the etched first insulation films 114a protrude from between portions of the etched second silicon nitride film pattern 110a.

[0039] The first insulation film 114 and the second silicon nitride film pattern 110 may be etched using a dry etching process or a chemical-mechanical

polishing process. In the drying etching process, the etching is performed so that the second silicon nitride film pattern 110 is etched more rapidly than the first insulation film 114. Preferably, an etching ratio between the first insulation film 114 and the second silicon nitride film pattern 110 is about 1:1 - 1:1.5. When a greater amount of the second silicon nitride film pattern 110 is etched as compared to the first insulation film 114, the second silicon nitride film pattern 110 may be over-etched so that a processing margin may be insufficient. In addition, when an etching rate of the first insulation film 114 is slower than that of the second silicon nitride film pattern 110, the time for etching the first insulation film 114 increases. As a result of the above-described dry etching process, portions of the etched first insulation film 114a protrude from the portions of the etched second silicon nitride film pattern 110a.

[0040] Alternately, a chemical-mechanical polishing process may be performed using a slurry for removing silicon nitride more rapidly than silicon oxide. Similar to the above dry etching process, the etching ratio between the first insulation film 114 and the second silicon nitride film pattern 110 is about 1:1 - 1:1.5 in the chemical-mechanical polishing process.

[0041] When the second silicon nitride film pattern 110 is etched to have a level upper surface, portions of the first insulation film 114 remain having heights higher than those of portions of the etched second silicon nitride film pattern 110a at peripheral portions of the etched second silicon nitride film pattern 110a. As a result, side portions of the etched second silicon nitride film pattern 110a are not exposed during the etching process forming the etched second silicon nitride film pattern 110a. Hence, side portions of the second silicon nitride film pattern 110a, which protect lateral portions of the conductive film pattern 103, are not etched during the etching process. Subsequent to this etching process, the etched second silicon nitride pattern 110a includes an etched nitride spacer 108a and an etched first silicon nitride film pattern 105b capping the conductive film pattern 103. In addition, during this etching process the nitride liner 112 is etched to have a level upper surface thereby forming an etched nitride liner 112a.

[0042] If upper portions of the first insulation film 114 and the second silicon nitride film pattern 110 are etched so that the second silicon nitride film pattern 110a has a level lower surface, portions of the first insulation film 114a are partially removed between the second silicon nitride film patterns

110a during the etching process. In addition, side portions of the second silicon nitride film pattern 110a are exposed, and then the side portions of the second silicon nitride film pattern 110a are partially removed as the portions of the first insulation film 114a are removed between the second silicon nitride film patterns 110a. As a result, the conductive film pattern 103 may not be capped with the second silicon nitride film pattern 110a because the second silicon nitride film pattern 110a is over-etched.

[0043] Accordingly, the etching process is preferably performed so that a width of the upper surface of the etched second silicon nitride film pattern 110a (W1) on the conductive pattern 103 is wider than that of an upper surface of the conductive pattern 103 (W2). In addition, a thickness of more than approximately 500 Å of the second silicon nitride film pattern 110a is preferably removed during the etching process. Thus, the shoulder portion of the second silicon nitride film pattern 110a is no longer rounded, and the overall height of the second silicon nitride film pattern 110a is reduced.

[0044] Referring to FIG. 2F, a second insulation film 116 is formed on the resultant structure including the etched second silicon nitride film pattern 110a having the level upper surface.

[0045] Since the etched first insulation film 114a includes silicon oxide having a good reflow-ability, and since the etched first insulation film 114a is filled in a space between the etched second silicon nitride film pattern 110a, the second insulation film 116 does not need to be formed using a material having a good reflow-ability since the second insulating film 116 is formed on a planarized surface. Hence, the second insulation film 116 is formed with a material comprised of tightly bonded atoms to protect the insulation films during successive processes. In particular, the atoms of the second insulation film 116 have tighter bonds that the atoms of the first insulation film 114.

[0046] More specifically, because the etched first and the second insulation films 114a and 116 may be primarily damaged during a rinsing process and the etched first and the second insulation films 114a and 116 are undesirably etched by a rinsing chemical, an etching failure may occur due to the rinsing chemical. Considering this problem, the second insulation film 116 is formed to have an etching rate slower than that of the first insulation film 114a. That is, the second insulation film 116 can be formed using a material different from the material of the first insulation film 114a, or the

second insulation film 116 can be formed through a process different from that of the first insulation film 114a. In particular, when the first insulation film 114 is comprised of BPSG, the second insulation film 116 may be composed of BPSG including boron (B) and phosphorus (P) ion concentrations lower than the concentrations of boron and phosphorous in the first insulation film 114. Alternatively, the second insulation film 116 may be formed by a high-density plasma chemical vapor deposition process or a plasma-enhanced chemical vapor deposition process.

[0047] Referring to FIG. 2G, portions of the second and the first insulation films 116 and 114a are etched to expose portions of the semiconductor substrate 100 positioned between the etched second silicon nitride film pattern 110a. This etching results the formation of a twice-etched second silicon nitride film pattern 110b, including a twice-etched nitride spacer 108b and a twice-etched first silicon nitride film pattern 105c capping the conductive film pattern 103, and an etched second insulation film 116a. Subsequently, a twice-etched nitride liner 112b remaining on the semiconductor substrate 100 is etched to form self-aligned contact holes 120.

[0048] More particularly, after a photoresist film is coated on the etched second insulation film 116a, the photoresist film is exposed and developed using a mask for forming a self-aligned contact hole, thereby forming a photoresist pattern (not shown) for opening a self-aligned contact region of the semiconductor substrate 100. The photoresist pattern has an open region and a mask region. The open region covers a space between the twice-etched second silicon nitride film pattern 110b and an edge portion of the upper surface of the twice-etched second silicon nitride film pattern 110b adjacent to the space. In addition, the mask region masks a portion of the upper surface of the twice-etched second silicon nitride film pattern 110b.

[0049] Subsequently, an anisotropic etching process for forming the self-aligned contact holes 120 is performed using the photoresist pattern as an etching mask to provide a high etching selectivity between silicon oxide and silicon nitride. The anisotropic etching process may be performed using a mixture of CHF_3, CF_4 and Ar. Using the anisotropic etching process, portions of the etched second insulation film 116a exposed in the open region of the photoresist pattern are primarily etched. When the portions of the etched second insulation film 116a are completely etched, portions of the

twice-etched first insulation film 114b and the twice-etched second silicon nitride film pattern 110b are simultaneously exposed. Then, portions of the twice-etched first insulation film 114b are selectively etched to expose the nitride liner 112b positioned between the twice-etched second silicon nitride film patterns 110b. When the twice-etched first insulation film 114b is etched a third time, the twice-etched second silicon nitride film pattern 110b is etched slower than the twice-etched first insulation film 114b in accordance with the etching selectivity between the second silicon nitride film pattern 110 and the first insulation film 114.

[0050] Subsequently, the photoresist pattern is removed by an ashing process after contact holes 120 exposing the semiconductor substrate 100 are formed between the twice-etched second silicon nitride film pattern 110b by etching the exposed twice-etched nitride liner 112b. Thus, between adjacent twice-etched second silicon nitride film pattern 110b the first insulation film 114 is completely removed, and the etched second insulation film 116a and the twice-etched second silicon nitride film pattern 110b are exposed through sidewalls of the contact holes 120.

[0051] As described above, the twice-etched second silicon nitride film pattern 110b has a level upper surface and a height of the twice-etched second silicon nitride film pattern 110b is decreased by approximately 500 Å, thereby reducing the generation of process failures generated during the etching process.

[0052] Hereinafter, a reduction of the likelihood of process failures will be described in detail according to a shape of the twice-etched second silicon nitride film pattern 110b.

[0053] As a height of the twice-etched second silicon nitride film pattern 110b decreases, an etched thickness is also reduced due to the etching selectivity between silicon nitride and silicon oxide while the contact holes 120 are formed through the self-aligning process. As a result, the etched thickness of the twice-etched second silicon nitride film pattern 110b is reduced during the etching of the twice-etched first and the etched second insulation films 114b and 116a. Thus, a process failure, for example an exposure of the conductive film pattern 103 in the twice-etched second silicon nitride film pattern 110b, may be prevented as predetermined portions of the twice-etched second silicon nitride film pattern 110b are etched. In addition,

another process failure, such as a contact non-opening, may be reduced in accordance with the reduction of the etched thickness during the self-aligning process.

[0054] Furthermore, the etching selectivity between the twice-etched second silicon nitride film pattern 110b and the twice-etched first and etched second insulation films 114b and 116a increases because the twice-etched second silicon nitride film pattern 110b has a level upper surface. Therefore, still another process failure, such as an over-etch of the twice-etched second silicon nitride film pattern 110b, may be prevented since the twice-etched second silicon nitride film pattern 110b is etched less when the etched first insulation film 114a is twice etched and the second insulation film 116 is first etched.

[0055] Though silicon oxide and silicon nitride may be etched under identical etching conditions, an etching selectivity between silicon oxide and silicon nitride may be generated depending on the structure including the silicon oxide and the silicon nitride. FIGS. 3A to 3C illustrate cross-sectional view structures including silicon oxide and silicon nitride. The structures are

etched to remove a portion of the silicon oxide so as to expose the silicon nitride.

[0056] FIG. 3A illustrates a structure including a silicon nitride layer, having a level upper surface, and a silicon oxide layer. FIG. 3B and FIG. 3C illustrate structures including a silicon nitride layer, having an uneven upper surface, and a silicon oxide layer.

[0057] It is experientially known that when a level silicon nitride film 200a and a level silicon oxide film 202a are formed on a substrate (not shown) as in FIG. 3A, an etching selectivity between the level silicon nitride film 200a and the level silicon oxide film 202a is higher than an etching selectivity between an uneven silicon nitride film 200b, 200c and a silicon oxide film 202b, 202c formed on the uneven silicon nitride film 200b, 200c, as may be seen in FIGS. 3B and 3C, respectively.

[0058] That is, when portions of the silicon oxide films 202b and 202c and the uneven silicon nitride films 200b and 200c, which are simultaneously exposed during an etching process, exist as shown in FIGS. 3B and 3C, the etching selectivity is lower as compared to a case in which one film between the silicon oxide film 202a and the silicon nitride film 200a is exposed only as

shown in FIG. 3A. In addition, in the etching process, the etching selectivity is further reduced in accordance with a reduction of an exposed area of the silicon nitride films 200b and 200c at a location 205 of FIG. 3B and 206 of FIG. 3C when the silicon oxide films 202b and 202c and the silicon nitride films 200b and 200c are simultaneously exposed. More specifically, as shown in FIG. 3B, when the silicon nitride film 200b has an uneven surface, the exposed area of the silicon nitride film 200b is greatly reduced at location 205 when the silicon oxide film 202b and the silicon nitride film 200b are simultaneously exposed. On the other hand, as shown in FIG. 3C, when the silicon nitride film 200c has a level surface, the exposed area of the silicon nitride film 200c is relatively increased at location 206 when the silicon oxide film 202c and the silicon nitride film 200c are simultaneously exposed.

[0059] In a conventional method for forming a semiconductor device, because the upper surface of the second silicon nitride film pattern has a round shape, as may be seen in FIG. 1C, the exposed area of the second silicon nitride film pattern is relatively small at the location where the silicon oxide film and the second silicon nitride film pattern are simultaneously exposed during the etching process. Hence, the exposed second silicon

nitride pattern is simultaneously and rapidly etched during the etching of the silicon oxide film. However, in the first embodiment of the present invention, the exposed area of the second silicon nitride pattern 110b is relatively wide at the location where the second silicon nitride pattern 110b and the insulation films 116a and 114b are simultaneously exposed during the etching process because the twice-etched second silicon nitride pattern 110b has a level upper surface. As a result, when the insulation films 116a and 114b are etched, the etching rate of the twice-etched second silicon nitride pattern 110b is slower than that in the conventional process. Thus, a process failure, such as an over-etch of the twice-etched second silicon nitride pattern 110b, may be prevented because the consumption of the etched second silicon nitride pattern 110a is reduced.

[0060] Referring back to FIG. 2G, the semiconductor substrate 100 including the contact holes is rinsed to remove polymers generated during the etching process, thereby forming self-aligned contact holes 120. The semiconductor substrate 100 is rinsed using a rinsing chemical. When the semiconductor substrate 100 is rinsed with the rinsing chemical, exposed films on the semiconductor substrate 100 are partially etched. In this case,

the twice-etched first insulation film 114b is not exposed on the semiconductor substrate 100 through a bottom surface or sidewall of the contact hole 120. Thus, an etching failure of the twice-etched first insulation film 114b due to the rinsing chemical may be prevented.

[0061] The first insulation film 114 is comprised only of a material having a good reflow-ability to fill the gap between the gate structures, and such material includes atoms bonded with weak bonds. Hence, when the semiconductor substrate 100 is rinsed with the rinsing chemical, the first insulation film 114 is rapidly etched since the atoms in the surface of the first insulation film 114 rapidly react with the rinsing chemical. In a case that the first insulation film 114 is partially etched, the twice-etched first insulation film 114b between the contact holes 120 does not have a stable structure. In addition, a bridge failure may occur by connecting one gate structure to an adjacent gate structure through the contact hole 120 due to the partially removed twice-etched first insulation film 114b. However, in the first embodiment of the present invention, the twice-etched first insulation film 114b is not exposed through a bottom surface or a sidewall of the contact hole 120, only the etched second insulation film 116a, which is slowly etched

against the rinsing chemical is exposed, so the above-mentioned problems may be prevented.

[0062] Referring to FIG. 2H, a conductive material is formed in the self-aligned contact hole 120 to form a contact 122.

[0063] According to the first embodiment of the present invention, process failures for forming a self-aligned contact hole may be prevented by utilizing an etching selectivity between silicon oxide and silicon nitride when the silicon nitride pattern enclosing the conductive film pattern has a level upper surface and a height of the silicon nitride pattern is reduced. In the first embodiment, any self-aligned contact hole positioned between adjacent conductive patterns may be formed using the above-described method even though an exemplary contact hole in the first embodiment is described as being formed between gate electrodes.

Second Embodiment

[0064] FIGS. 4A to 4E illustrate cross-sectional views of stages in a method for forming a self-aligned contact hole of a semiconductor device according to a second embodiment of the present invention. In FIGS. 4A to 4E, the

same reference numerals are used for elements common to the first embodiment.

[0065] The second embodiment is distinct from the first embodiment in that height difference between a first insulation film and a silicon nitride pattern is not generated during a process for forming the silicon nitride pattern having a level upper surface by successively etching the first insulation film and the silicon nitride pattern.

[0066] Referring to FIG. 4A, a first insulation film 114 covering a second silicon nitride pattern 110 is formed in the same manner as described in connection with FIGS. 2A to 2D.

[0067] Referring to FIG. 4B, upper portions of the first insulation film 114 and the second silicon nitride pattern 110 are successively etched so that the etched second silicon nitride pattern 110a has a level upper surface. As a result of the successive etching in the second embodiment, which still may be a dry etching process or a chemical-mechanical process, no height difference is generated between the first insulation film 114 and the etched second silicon nitride pattern 110a. In the etching process, when the second silicon nitride pattern 110 is etched to have the level upper surface,

the etched first insulation film 114a remains at a peripheral portion of the etched second silicon nitride pattern 110a exposed during the etching process so that the etched first insulation film 114a has a height identical to that of the etched second silicon nitride pattern 110a. Hence, because a side portion of the etched second silicon nitride pattern 110a is not exposed during the etching process, the side portion of the etched second silicon nitride pattern 110a is not etched, thereby securely protecting a conductive film pattern 103. With the etching process, a width of the upper surface of the second silicon nitride pattern 110a on the conductive film pattern 103 is at least wider than that of an upper surface of the conductive film pattern 103.

[0068] Referring to FIG. 4C, a second insulation film 116 is formed on the resultant structure including the etched second silicon nitride pattern 110a having the level upper surface. The second insulation film 116 is formed using a material including atoms more tightly bonded than the atoms of the first insulation film 114, so the second insulation film 116 is not readily consumed during successive processes.

[0069] Referring to FIG. 4D, predetermined portions of the second insulation film 116 and the etched first insulation film 114 are etched to expose portions

of a semiconductor substrate 100 between the twice-etched second silicon nitride patterns 110b. Then, the twice-etched nitride liner 112b formed on the semiconductor substrate 100 is etched to primarily form self-aligned contact holes 120.

[0070] Subsequently, the self-aligned contact holes 120 are completely formed after rinsing the semiconductor substrate 100 to remove polymers generated during the etching process. At that time, the twice-etched first insulation film 114b is not exposed through a bottom surface and a sidewall of the contact hole 120, so process failures due to an etch of the twice-etched first insulation film 114b with a rinsing chemical may be prevented.

[0071] Referring to FIG. 4E, a contact 122 is formed by filling a conductive material in the self-aligned contact hole 120.

[0072] As described above, according to the present invention, process failures generated during a formation of a self-aligned contact hole may be prevented because a nitride pattern capping a conductive film pattern is not consumed. Therefore, a reliability of a semiconductor device may be enhanced and a yield of a manufacturing process for the semiconductor device may also be improved.

[0073] Preferred embodiments of the present invention have been disclosed herein and, although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. Accordingly, it will be understood by those of ordinary skill in the art that various changes in form and details may be made without departing from the spirit and scope of the present invention as set forth in the following claims.